Remarks

The Final Office Action mailed September 14, 2001 has been received and reviewed. Claims 27, 32 and 36 have been amended, and new claims 39-44 have been added. Therefore, claims 27-44 are pending.

The 35 U.S.C. §102 Rejections

Claims 27-35

The Examiner rejected claims 27-35 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,122,923 to Matsubara et al. (hereinafter "Matsubara"). Specifically, the Examiner alleges that Matsubara discloses a thin-film capacitor comprising a lower electrode, a dielectric layer, and an upper electrode. The lower electrode is alleged to be made from $RuSi_2$ and may consist of layers of ruthenium, ruthenium oxide, ruthenium oxide, ruthenium silicide and stacked structures.

Applicants have amended claims 27 and 32 to more clearly define the claimed subject matter. Insofar as the rejection is applied to claims 27 and 32, as clarified, Applicants respectfully traverse the rejection of claims 27-35.

Matsubara recites a thin-film capacitor with a silicon substrate, an insulating silicon oxide layer, a lower electrode, a dielectric layer of $BaTiO_3$ and an upper electrode of aluminum layer stacked in sequence from bottom to top (Col. 3, lines 42-47). Lower electrode layer is formed by a DC magnetron sputtering technique using a target of sintered Ru or $RuSi_2$ (Col. 3, lines 53-56).

Applicants' teach a semiconductor device structure comprising a substrate assembly that includes a surface, and a chemical vapor deposited diffusion barrier layer of $RuSi_x$ over at least a portion of the surface, where x is in the range of about 0.01 to about 10.

For a claim to be anticipated under 35 U.S.C. § 102(b), each and every element of the claim must be found in a single prior art reference. Applicants respectfully submit that Matsubara fails to anticipate the subject matter recited in claims 27-35. For example, Matsubara

recites a lower electrode layer, but fails to teach a diffusion barrier layer, as recited in claims 27-35.

In addition, Matsubara clearly fails to teach a semiconductor device structure that includes a chemical vapor deposited diffusion barrier layer of $RuSi_x$ over at least a portion of a surface. Matsubara describes a sputtered $RuSi_2$ electrode layer and not a chemical vapor deposited diffusion barrier layer.

A chemical vapor deposited diffusion barrier layer according to the present invention is different than a layer sputtered such as described by Matsubara. For example, a sputter coated layer, particularly with respect to high aspect ratio structures, provides different coverage thereon when compared to a chemical vapor deposited layer. For example, a sputtered layer at the edge of a contact hole tends to be particularly thick, reducing the opening of the holes disproportionately or, for example, sputtered material may not reach the bottom of the contact holes.

In contrast, a chemical vapor deposited film provides a highly conformal layer within deep contacts and other openings such as for lower electrodes of storage cell capacitors. (Applicants' disclosure page 9, lines 15-17). These highly conformal layers relative to high aspect ratio structures are generally not possible with sputter coating. Thus, the structures recited in claims 27-35, including chemical vapor deposited layers, are physically structurally and patentably distinct from those recited in Matsubara which include sputtered layers.

As such, claims 27-35 are not anticipated by Matsubara et al. Applicants respectfully request reconsideration and withdrawal of the rejection.

Claims 36-38

The Examiner also rejected claims 36-38 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,491,365 to Chin et al. (hereinafter "Chin"). Specifically, the Examiner alleges that Chin discloses an integrated circuit device comprising a substrate, contact, and contact diffusion barrier.

Applicants have amended claim 36 to more clearly define the claimed subject matter. Insofar as the rejection is applied to claim 36, as clarified, Applicants respectfully traverse the rejection of claims 36-38.

Chin recites a contact diffusion barrier that is formed from "[a] layer of low resistivity materials . . . and a second material . . . implanted into the low resistivity material . . ." where "[t]he low resistivity and implanted materials are selected to form a conductive diffusion barrier . . . that resists diffusion from an overlying metal contact into the semiconductor" (Col. 2, lines 38-46). "The implantation is preferably accomplished by plasma etching" (Col. 2, lines 53-54). Chin states that "both the low resistivity material and the implanted material include a transition metal, with the transition metals from the two source materials forming a composite transition metal diffusion barrier" (Col. 3, lines 32-35). Alternatively, "the low resistivity layer . . . includes a transition metal, but a non-transition metal is implanted into it" to form the diffusion barrier (Col 3, lines 56-67).

Applicants' teach an integrated circuit structure comprising a substrate assembly that includes at least one active device and a silicon containing region, and an interconnect formed relative to the at least one active device and the silicon containing region, the interconnect including a chemical vapor deposited diffusion barrier layer formed of $RuSi_x$ on at least a portion of the silicon containing region, where x is in the range of about 0.01 to about 10.

For a claim to be anticipated under 35 U.S.C. § 102(b), each and every element of the claim must be found in a single prior art reference. Applicants respectfully submit Chin fails to anticipate the subject matter recited in claims 36-38. For example, Chin recites a contact diffusion barrier formed by implanting a component of the barrier material into a resistivity material to establish a third material that comprises the barrier (Chin, Col. 3, lines 21-25). Chin indicates that "[a] wide variety of materials can be used to implement the invention . . . [where] both the low resistivity material and the implanted material include a transition metal, with the transition metals from the two source materials forming a composite transition metal diffusion barrier" (Chin, Col. 3, lines 30-34). Silicides of the transition metals, such as $RuSi_2$, are preferred for the low resistivity material because they establish a good contact to the underlying

semiconductor material (Chin, Col. 3, lines 34-37). "When implanted into the low resistivity layer under the proper conditions . . . a composite transition metal which combines the implant material and the transition metal from the low resistivity layer is formed; such composite transition metals are effective diffusion barriers" (Chin, Col. 3, lines 43-48). The diffusion barrier is, therefore, not $RuSi_2$ *per se*, but a composite transition metal "formed from two different transition metals" (Chin, Col. 3, lines 51-52). Thus, Chin fails to teach a chemical vapor deposited diffusion barrier layer formed of $RuSi_x$ on at least a portion of the silicon containing region.

As such, claims 36-38 are not anticipated by Chin. Applicants respectfully request reconsideration and withdrawal of the rejection.

The 35 U.S.C. §103 Rejection

The Examiner rejected claims 27-35 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,005,102 to Larson (hereinafter "Larson") in view of Chin. Specifically, the Examiner alleges that Larson discloses a capacitor comprising a bottom electrode, a dielectric, and a top electrode. The bottom electrode is alleged to comprise a diffusion barrier and layers. The Examiner recognizes that Larson does not disclose a diffusion barrier layer of $RuSi_2$. However, the Examiner alleges that Chin states that $RuSi_2$ is a preferable material for a diffusion barrier and that it would have been obvious to one of skill in the art to use such a material since it establishes good contact to an underlying semiconductor material as stated in Chin.

Applicants have amended claims 27 and 32 to more clearly define the claimed subject matter. Insofar as the rejection is applied to claims 27 and 32, as clarified, Applicants respectfully traverse the rejection of claims 27-35.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally the prior art references must teach or suggest all the claim limitations.

The cited references do not teach or suggest all the claim limitations of the claims. For example, the cited references do not describe a chemical vapor deposited diffusion barrier layer formed of $RuSi_x$. Rather, Larson (as acknowledged by the Examiner) does not describe a $RuSi_x$ diffusion barrier layer at all, and further, Chin describes a barrier layer formed by implanting a component of the barrier into a lower resistivity material to establish a composite metal barrier (as discussed above).

Further, there is no teaching or suggestion to combine such references to provide a chemical vapor deposited diffusion barrier layer formed of $RuSi_x$. Rather, Chin actually teaches away from use of such a method of forming a $RuSi_x$. For example, as specifically described therein, a barrier layer is formed by implanting a component of the barrier into a lower resistivity material to establish a material that comprises the diffusion barrier. This is specifically performed to alleviate problems of other formation methods, e.g., sputtering. To form the diffusion barrier layer of Chin using chemical vapor deposition or any other method would be destroying the function of the layer formed in Chin.

As such, the pending claims are not obvious over the combination of Chin and Larson. Applicants respectfully request reconsideration and withdrawal of the rejection.

Summary

In view of the above amendments and remarks, reconsideration and withdrawal of the rejections are respectfully requested. It is respectfully submitted that the pending claims are in condition for allowance and notification to that effect is respectfully requested. The Examiner is invited to contact Applicants' Representatives, at the below-listed telephone number, if it is believed that prosecution of this application may be assisted thereby.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR §1.8:
The undersigned hereby certifies that this paper is being deposited with the United States Postal Service as first class mail, in an envelope addressed to: Assistant Commissioner for Patents, **BOX AF**, Washington, D.C. 20231 on this 14th day of November, 2001.

By: _____
Name: Mark J. Gebhardt

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APPENDIX A - CLAIM AMENDMENTS
INCLUDING NOTATIONS TO INDICATE CHANGES MADE
Serial No.: 09/603,132
Docket No.: 150.00650102

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Amendments to the following are indicated by underlining what has been added and bracketing what has been deleted.

In the Claims

For convenience, all pending claims are shown below.

27. (Twice Amended) A semiconductor device structure, the structure comprising:

a substrate assembly including a surface; and

a chemical vapor deposited diffusion barrier layer over at least a portion of the surface, wherein the diffusion barrier layer is formed of $RuSi_x$ [using chemical vapor deposition], where x is in the range of about 0.01 to about 10.

28. The structure of claim 27, wherein x is in the range of about 1 to about 3.

29. The structure of claim 28, wherein x is about 2.0.

30. The structure of claim 27, wherein the at least a portion of the surface is a silicon containing surface and further wherein the structure includes one or more additional conductive layers over the diffusion barrier layer formed of at least one of a metal and a conductive metal oxide.

31. The structure of claim 30, wherein the one or more conductive layers are formed from materials selected from the group of RuO_2, RhO_2, MoO_2, IrO_2, Ru, Rh, Pd, Pt, and Ir.

32. (Twice Amended) A capacitor structure comprising:

a first electrode;

a high dielectric material on at least a portion of the first electrode; and

a second electrode on the dielectric material, wherein at least one of the first and second electrode comprises a chemical vapor deposited diffusion barrier layer formed of $RuSi_x$ [using chemical vapor deposition], where x is in the range of about 0.01 to about 10.

33. The structure of claim 32, wherein x is in the range of about 1 to about 3.

34. The structure of claim 32, wherein the first electrode comprises a diffusion barrier layer, wherein the diffusion barrier layer of the first electrode is formed on at least a portion of a silicon containing region, and further wherein the first electrode comprises one or more additional conductive layers formed over the diffusion barrier layer, the one or more additional conductive layers formed of at least one of a metal and a conductive metal oxide.

35. The structure of claim 34, wherein the one or more additional conductive layers are formed from materials selected from the group of RuO_2, RhO_2, MoO_2, IrO_2, Ru, Pt, and Ir.

36. (Twice Amended) A integrated circuit structure comprising:

a substrate assembly including at least one active device and a silicon containing region; and

an interconnect formed relative to the at least one active device and the silicon containing region, the interconnect including a chemical vapor deposited diffusion barrier layer on at least a portion of the silicon containing region, wherein the diffusion barrier layer is formed of $RuSi_x$ [using chemical vapor deposition], where x is in the range of about 0.01 to about 10.

37. The structure of claim 36, wherein x is in the range of about 1 to about 3.

38. The structure of claim 36, further comprising a conductive contact material formed relative to the diffusion barrier layer.

39.(New) The structure of claim 27, wherein the surface of the substrate assembly defines an opening, where the diffusion barrier layer is on the surface defining the opening.

40.(New) The structure of claim 39, wherein the opening has an aspect ratio greater than about 1.

41.(New) The capacitor structure of claim 32, wherein the capacitor structure includes a surface defining an opening, and wherein the first electrode comprises a diffusion barrier layer formed on the surface defining the opening.

42.(New) The capacitor structure of claim 41, wherein the opening has an aspect ratio greater than about 1.